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Substitute for form 1449A/PTO				Application Number	10/066,456
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Filing Date	1/31/02
(use as many sheets as necessary)				First Named Inventor	Steven Teig, et al.
				Group Art Unit	2825
				Examiner Name	B. Tat
Sheet	1	of	2	Attorney Docket Number	SPLX.P0099

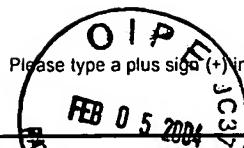
U.S. PATENT DOCUMENTS

Examiner* Initials	Cite No. ¹	U.S. Patent Document Number		Date of Publication MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	2002/0157063	A1	10-24-2002	Besson	
	2.	2002/0178432	A1	11-28-2002	Kim et al.	
	3.	2003/0145288	A1	07-31-2003	Wang et al.	
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	21.	6,543,037	B1	04-01-2003	Limqueco et al.	

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	23.	6,618,835	B1	09-09-2003	Garlapati et al.	

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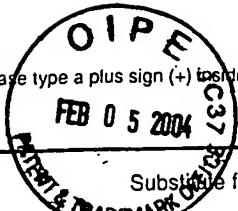
Examiner* Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ⁶
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		Number	Kind Code ² (if known)			
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	2. 5,519,630			05-21-1996	Nishiyama et al.	
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	18. 6,473,884			10-29-2002	Ganai et al	
	19. 6,496,972	B1		12-17-2002	Segal	
	20. 6,523,156	B2		02-18-2003	Cirit	
	21. 6,574,779	B2		06-03-2003	Allen et al.	

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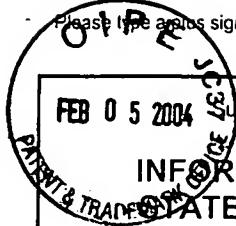
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	23.	Devadas, S. et al., Synthesis and Optimization for Robustly Delay-fault Testable Combinational Logic Circuits, Design Automation Conference, 1990, 27 th ACM/IEEE, June 24-28, 1990, pp.221-227.	
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RELATED U.S. PATENT APPLICATIONS

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		Serial Number				
	1.	10/062,017		Steven Teig & Asmus Hetzel	01-31-02	
	2.	10/061,459		Steven Teig & Asmuz Hetzel	01-31-02	
	3.	10/062,014		Steven Teig & Asmus Hetzel	01-31-02	
	4.	10/062,044		Steven Teig & Asmuz Hetzel	01-31-02	
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	6.	10/066,188		Steven Teig & Asmus Hetzel	01-31-02	
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	8.	10/061,474		Steven Teig & Asmus Hetzel	01-31-02	
	9.	10/061,719		Steven Teig & Asmus Hetzel	01-31-02	
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	12.	5,649,165		Jain et al.	07-15-97	
	13.	6,301,687	B1	Jain et al.	10-09-01	

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OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

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	15.	Henrik Reif Andersen, An Introduction to Binary Decision Diagrams, October 1997 (minor revisions April 1998), 36 pp.
	16.	Jerry Burch and David Long, Efficient Boolean Function Matching, Proc. ICCAD 1992, 408-411.
	17.	John Fishburn, A Depth-Decreasing Heuristic for Combinational Logic; or How to Convert Ripple-Carry Adder into a Carry-Lookahead Adder or Anything In-Between, Proceedings of the 27 th Design Automation Conference, 361-364, 1990.
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	19.	Kurt Keutzer, DAGON: Technology Binding and Local Optimization by DAG Matching, Proceedings of the 24 th Design Automation Conference, 341-347, 1987
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